REMARKS

As of the Final Office Action mailed April 18, 2003 for the parent patent application (Serial No. 09/994, 233), Claims 1 - 20 were pending and rejected. . Claims 1, 10, and 17 have been amended. Claims 13 and 14 have been cancelled. This amendment is filed in conjunction with a request for continued examination and traverses the Examiner's rejections to the Final Office Action.

1. Claims 1-9 were rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (U.S. Patent No. 6,433,586 B2).

Amended Claim 1 has among other features: a cross coupled circuit having a cross coupled transistor configured to continuously receive power from a positive power supply voltage. In FIG. 9 of Ooishi the cross-coupled circuit having transistors PQ3 and PQ4 is connected to positive power supply PS1 via transistor TG2, which is periodically turned off and on. Thus Ooishi neither discloses nor suggests a cross coupled circuit having a cross coupled transistor configured to continuously receive power from a positive power supply voltage. And claim 1 should be allowable for at least this reason.

Claims 2-9 being dependent on claim 1 should be allowable for at least the same reasons claim 1 is allowable.

2. Claims 10-12 were rejected under 35 U.S.C. 102(b) as being anticipated by Hwang et. al. (U.S. Patent No. 5,777,491).

Amended Claim 10 has among other features: another transistor having a first current-handling terminal connected to the first output terminal, a second current-handling terminal connected to the second output terminal, and a control terminal having a clock signal. Hwang neither discloses nor suggests this feature and claim 10 should be allowable for at least this reason.

In addition, although Claim 10 incorporates the limitations of Claims 13 and 14, Claim 10 is not obvious under 35 U.S.C. 103(a) in view of Hwang combined with Choe (U.S. Patent No. 6,373,292). Choe in FIG. 2 has a transistor 56 coupled between output terminals 58 and 60, but does not have a transistor with a control terminal connected to an input terminal and a current handling terminal directly connected to VSS. The current handling terminal in Choe is connected via transistor 52 to ground. Transistors 56 and 52 work in concert and are alternatively on and off depending on the clock and its complement (col. 2, line 51 to col. 3, line 4). The removal of transistor 52 in Choe in order to combine Choe with Hwang would change the principle of operation of the circuit of Choe and hence the references cannot be combined. Thus claim 10 is not obvious and should be allowable.

Claims 11-12 and 15 -16 being dependent on claim 10 should be allowable for at least the same reasons claim 10 is allowable.

3. Claims 17-20 were rejected under 35 U.S.C. 103(a) as being obvious in view of Applicants' admitted prior art in view of Ooishi.

Amended Claim 17 has among other features: a first flip-flop having a cross coupled circuit having a cross coupled transistor directly connected to a positive power supply voltage. In FIG. 9 of Ooishi the cross-coupled circuit having transistors PQ3 and PQ4 is connected to positive power supply PS1 via transistor TG2. Thus Ooishi neither discloses nor suggests a cross coupled circuit having a cross coupled transistor directly connected to a positive power supply. Hence, replacing the flip-flops 110 of FIG. 1 of the application, as the Examiner suggests, with the Flip-flop 12 in FIG. 9 of Ooshi does not meet all the limitations of Claim 17 and claim 17 should be allowable for at least this reason.

Claims 18-20 being dependent on claim 17 should be allowable for at least the same reasons claim 17 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 17. 2003.

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